TRANSITION SYSTEM TO LOW POWER CONSUMPTION STATE

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Abstract

PURPOSE:To eliminate the disturbance of other task execution by bringing the computer system to the standby mode when the absence of a task to be executed is detected in the system applying multi-task processing.
CONSTITUTION:A computer system is added with a program memory 1, a program counter (PC) 2, an instruction decoder 3, a peripheral equipment 4, a clock generator 5, a data memory 6, a decision circuit 7, an AND gate 8 and a latch 21 with inverter, the instruction decoder 3 activates each signal line for the system operation. In this case, a clock is fed to the peripheral equipment 4 and the PC 2 via the AND gate 8 and when the output 20 of the latch 21 is inactive, the mode is brought into the standby mode where the peripheral equipment 4 is stopped. Further, the standby mode continues until the latch state is released.